

Noah Kanovsky

Mountain View, CA

240-393-7128 (m)
noahkanovsky@gmail.com

OBJECTIVE

I seek full time employment or projects as a Senior FPGA Engineer. I am highly proficient in the design of FPGAs, drivers, embedded software, and real-time applications.

EMPLOYMENT

VisionMap – Mapping Systems Senior FPGA Engineer

August 2008 – September 2009

- Designed and implemented Xilinx Virtex 5 FPGA. Integrated Xilinx MIG and Endpoint Block Plus for PCI Express. Designed and implemented scatter gather PCIe core. Designed and implemented PCIe WDM driver. Ported and optimized C algorithm to Verilog. Manually instantiated Xilinx primitives. Wrote C benchmarking and verification code for FPGA. Integrated fully functional system for demo.
- Re-designed and implemented Lattice SC/M FPGA in VHDL. Interfaced with Analog Devices ADV212, PLX local bus, Lattice DDR2 controller, Camera Link, and various embedded peripherals. Built FPGAs from schematic design to guarantee proper implementation. Worked with project managers on board level issues. Wrote C benchmark and verification code for FPGA designs.
- ❖ **At VisionMap, I implemented designs in record time, while providing the company with clean modular code and solving long-standing bugs and performance issues.**
- ❖ **I resigned from VisionMap to return to the United States.**

Mango DSP – Multi DSP & Security Systems Manager of Infrastructures Senior Embedded Software and FPGA Engineer

February 2001 – July 2008

- Wrote BSPs for embedded DSP / GPP systems. Read chip datasheets to properly design and implement interfaces. Designed software for many peripherals including EDMA, Timers, GPIOs, PCI, EMIFA/B, Cache, SPI, I2C, and Ethernet. Designed and implemented PCI and memory drivers for Windows, Solaris, Linux, VxWorks, and embedded operating systems.
- Researched and solved TI Codec Engine implementation issues. Trained other engineers in using TI Codec Engine and TI DaVinci peripherals. Worked with 3rd party codec suppliers on integration and debugging of TI DaVinci codecs.
- Designed and implemented Lattice MachXO FPGA for multi-DSP security platform. Implemented full FPGA with multiple UARTs, DSP to DSP communication, and various other components.
- Designed and implemented Altera Stratix II FPGA for multi-DSP encoding and decoding platform. Interfaced with client's pixel bus. Performed color space conversions. Implemented high speed DMA bus between FPGA and TI C64xx EMIF bus.
- Rewrote all modules in Altera Stratix II FPGA for standalone security platform. Solved stability and performance issues. Brought down resource usage and compilation time.
- Mentored and trained FPGA and software engineers.
- Implemented **many** other projects on various platforms & environments.
- ❖ **I was considered the technical "guru", being the go-to guy for all high priority issues in software and FPGAs, and having my expertise relied upon by the entire company.**
- ❖ **I resigned from Mango DSP to relocate to Tel Aviv, Israel.**

TECHNICAL SKILLS

Development languages:

- VHDL
- Verilog
- C
- C++ (proficient)

Development environments:

- Xilinx ISE
- Altera Quartus II
- Lattice ispLever
- Mentor Graphics ModelSim
- Microsoft Visual Studio, WDK (DDK)
- Texas Instrument Code Composer
- Wind River Tornado
- GCC, GDB

Chip families:

- Xilinx Virtex 5
- Lattice SC/M, MachXO
- Altera Stratix II, Cyclone
- TI C64xx, DM64x, DM644x (DaVinci)
- Freescale PowerPC
- Intel Pentium II

HDL interfaces:

- PCI Express (TLP and up)
- Camera Link
- UART (RS232 / RS485 / RS422)
- TI C6xxx DSP EMIF / HPI
- PLX local bus
- DDR2
- SMB / SPI / I2C
- RGB Pixel Bus

Software interfaces:

- PCI / PCI Express
- SPI / I2C / 1 Wire
- RTC / Watchdog
- TI DSP peripherals
- NOR FLASH
- UART (RS232 / RS485 / RS422)

EDUCATION

Yeshiva University - New York, NY - January 2001
Bachelor of Arts - magna cum laude - Computer Science

PERSONAL

Native US Citizen
Professional and personal references available upon request
LinkedIn URL: <http://www.linkedin.com/in/nkanovsky>
Website URL: <http://nkcorner.com/resume.php>

OPEN SOURCE PROJECTS

VHDL File-based CPU Emulator: http://www.opencores.org/project,vhdl_cpu_emulator
Password Security Solution <http://code.google.com/p/secureyourpassword/>